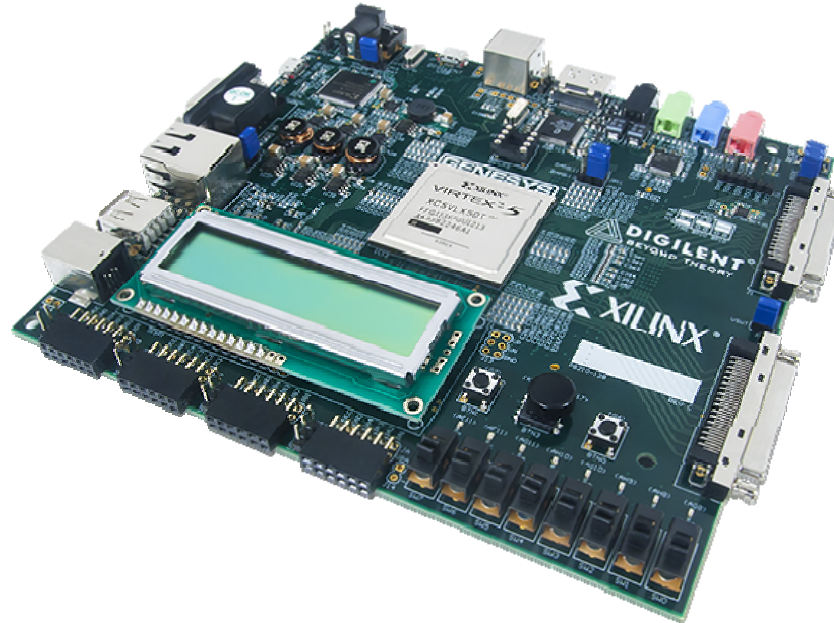
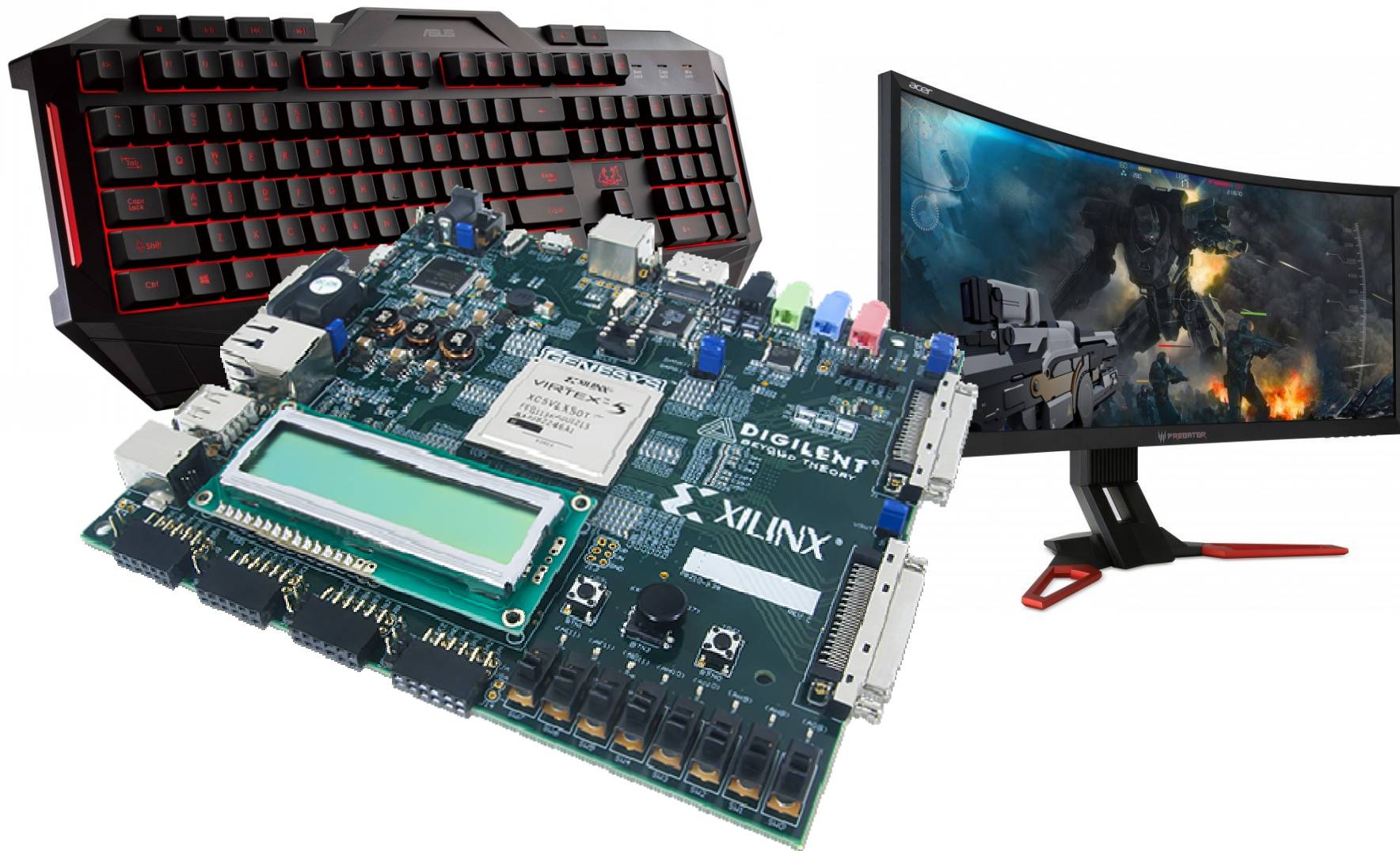


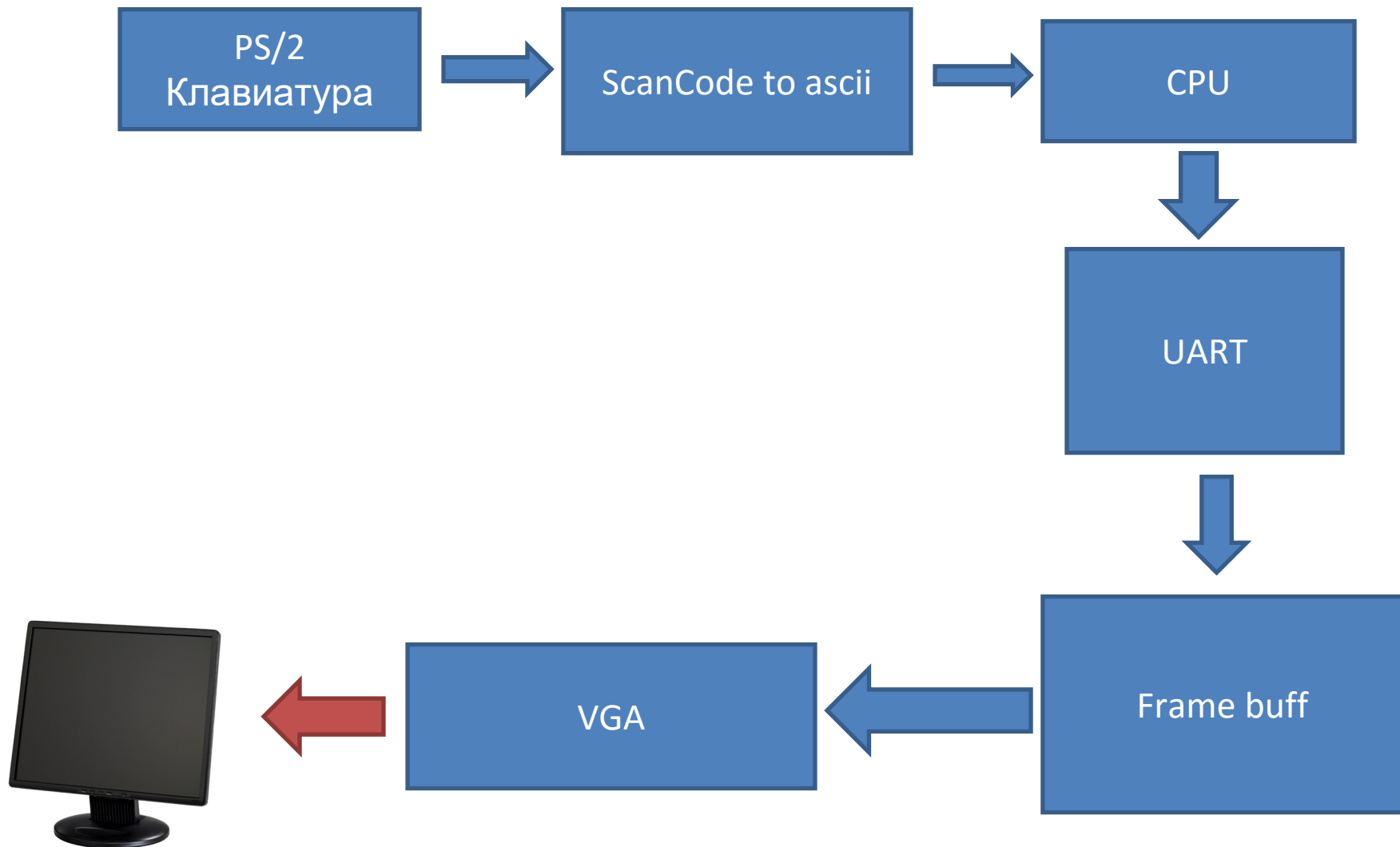
Реализация терминала на основе PS/2 клавиатуры и VGA/HDMI



Работу выполнил студент 2 курса Ким Андрей



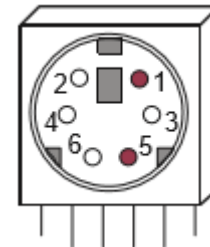
- [Xilinx Virtex-5](#) LX50T FPGA in a 1136-pin BGA package
- 256Mbyte DDR2 SODIMM with 64-bit wide data
- 32Mbyte Numonyx™ StrataFlash™ for configuration and user-data storage
- 100 MHz fixed oscillator and (up to) 400 MHz programmable clock generator
- Real time power monitors on all power rails
- Ships with a 20W power supply, USB cable, and protective plexiglass covers
- 10/100/1000 Ethernet PHY and RS-232 serial port
- Multiple USB2 ports for programming, data transfer, and hosting applications
- HDMI video with resolution up to 1600x1200 & 24-bit color
- AC-97 Codec with 48 KHz sampling and line-in, line-out, microphone and headphone ports
- GPIO includes 8 LEDs, 2 buttons, two-axis navigation switch, 8 slide switches, and a 16x2 character LCD
- 112 FPGA I/Os routed to expansion connectors (two high-speed parallel VHDC connectors and four 8-pin headers)
-

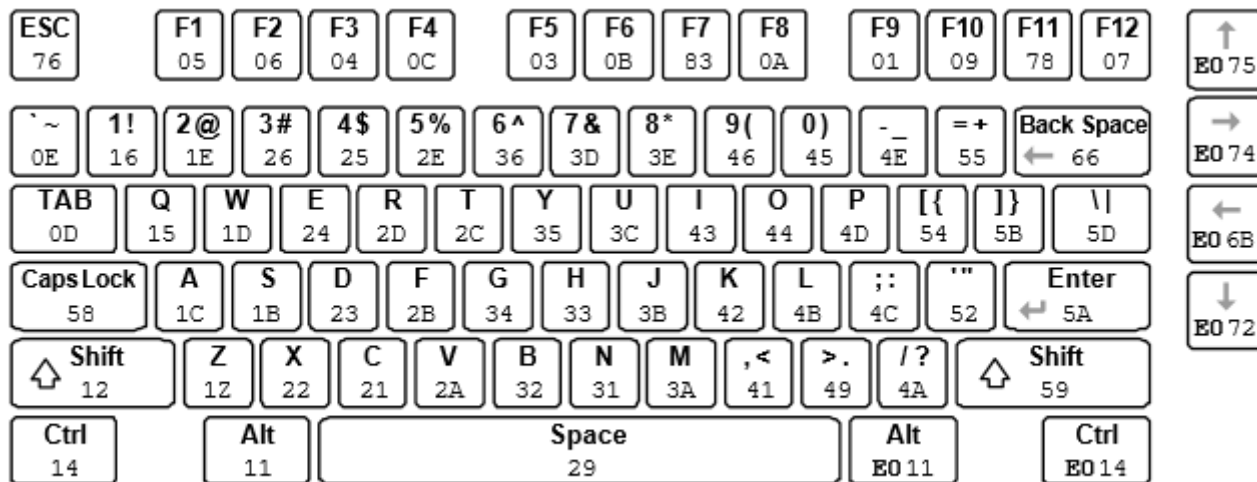


PS/2



PS/2 DIN Pin	Signal	FPGA Pin
1	DATA (PS2D)	M15
2	Reserved	—
3	GND	GND
4	Voltage Supply	—
5	CLK (PS2C)	M16
6	Reserved	—

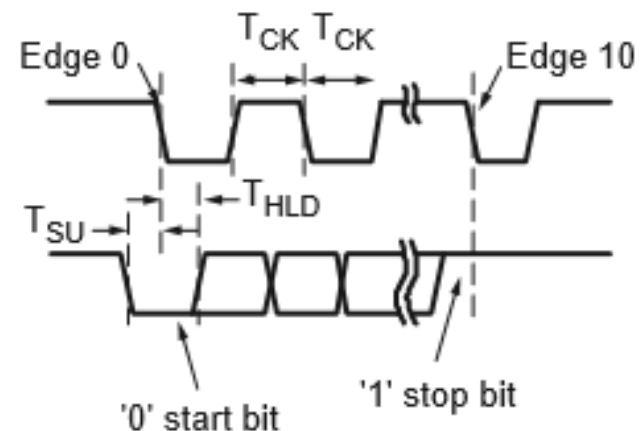




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CLK (PS2C)

DATA (PS2D)



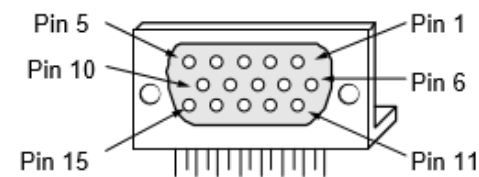
Dec	Hx	Oct	Char	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr	Dec	Hx	Oct	Html	Chr
0	0	000	NUL (null)	32	20	040	 	Space	64	40	100	@	@	96	60	140	`	`
1	1	001	SOH (start of heading)	33	21	041	!	!	65	41	101	A	A	97	61	141	a	a
2	2	002	STX (start of text)	34	22	042	"	"	66	42	102	B	B	98	62	142	b	b
3	3	003	ETX (end of text)	35	23	043	#	#	67	43	103	C	C	99	63	143	c	c
4	4	004	EOT (end of transmission)	36	24	044	$	\$	68	44	104	D	D	100	64	144	d	d
5	-	---		--	--	---			--	--	---		E	101	65	145	e	e
6	ESC76 F105F206F304F40C F503F60BF783F80A F901F109F1178F1207 ↑EO75												F	102	66	146	f	f
7	~OE1!162@1E3#264\$255%2E6^367&3D8*3E9(460)45-4E=+55Back Space←66 →EO74												G	103	67	147	g	g
8	TAB0DQ15W1D E24R2D T2C Y35U3C I43O44P4D [{54}]5B \5D ←EO6B												H	104	68	150	h	h
9	CapsLock58A1C S1B D23 F2B G34 H33 J3B K42 L4B ;:4C '"52Enter←5A ↓EO72												I	105	69	151	i	i
10	↑Shift12Z12X22C21V2AB32N31M3A,<41>49/?4AShift59												J	106	6A	152	j	j
11	Ctrl14Alt11Space29AltEO11CtrlEO14												K	107	6B	153	k	k
12													L	108	6C	154	l	l
13													M	109	6D	155	m	m
14													N	110	6E	156	n	n
15													O	111	6F	157	o	o
16													P	112	70	160	p	p
17													Q	113	71	161	q	q
18													R	114	72	162	r	r
19													S	115	73	163	s	s
20													T	116	74	164	t	t
21	15	025	NAK (negative acknowledge)	53	35	065	5	5	85	55	125	U	U	117	75	165	u	u
22	16	026	SYN (synchronous idle)	54	36	066	6	6	86	56	126	V	V	118	76	166	v	v
23	17	027	ETB (end of trans. block)	55	37	067	7	7	87	57	127	W	W	119	77	167	w	w
24	18	030	CAN (cancel)	56	38	070	8	8	88	58	130	X	X	120	78	170	x	x
25	19	031	EM (end of medium)	57	39	071	9	9	89	59	131	Y	Y	121	79	171	y	y
26	1A	032	SUB (substitute)	58	3A	072	:	:	90	5A	132	Z	Z	122	7A	172	z	z
27	1B	033	ESC (escape)	59	3B	073	;	:	91	5B	133	[	[	123	7B	173	{	{
28	1C	034	FS (file separator)	60	3C	074	<	<	92	5C	134	\	\	124	7C	174	|	
29	1D	035	GS (group separator)	61	3D	075	=	=	93	5D	135	]	]	125	7D	175	}	}
30	1E	036	RS (record separator)	62	3E	076	>	>	94	5E	136	^	^	126	7E	176	~	~
31	1F	037	US (unit separator)	63	3F	077	?	?	95	5F	137	_	_	127	7F	177		DEL

VGA



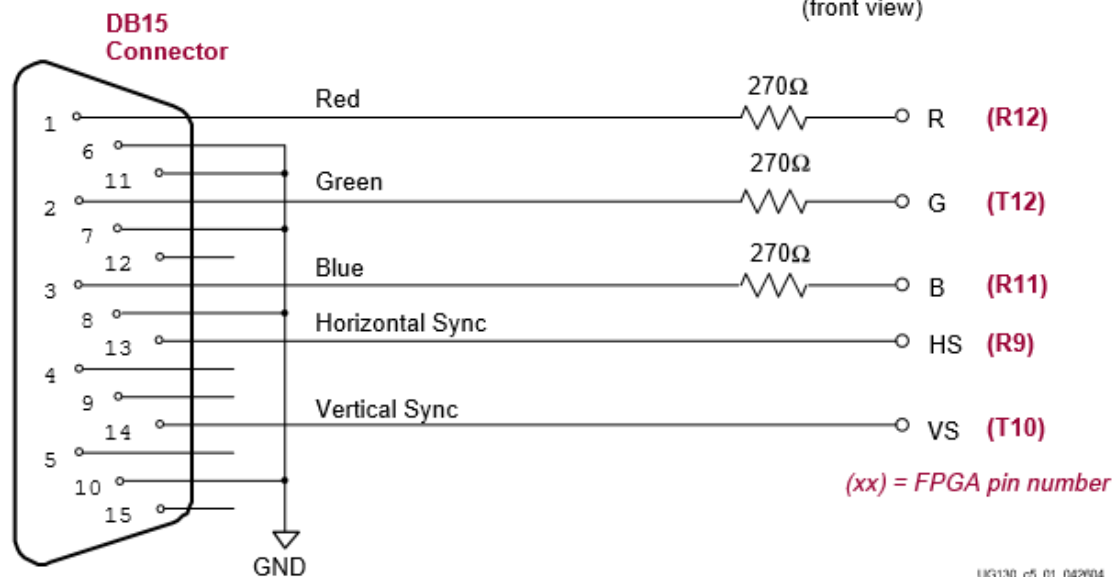


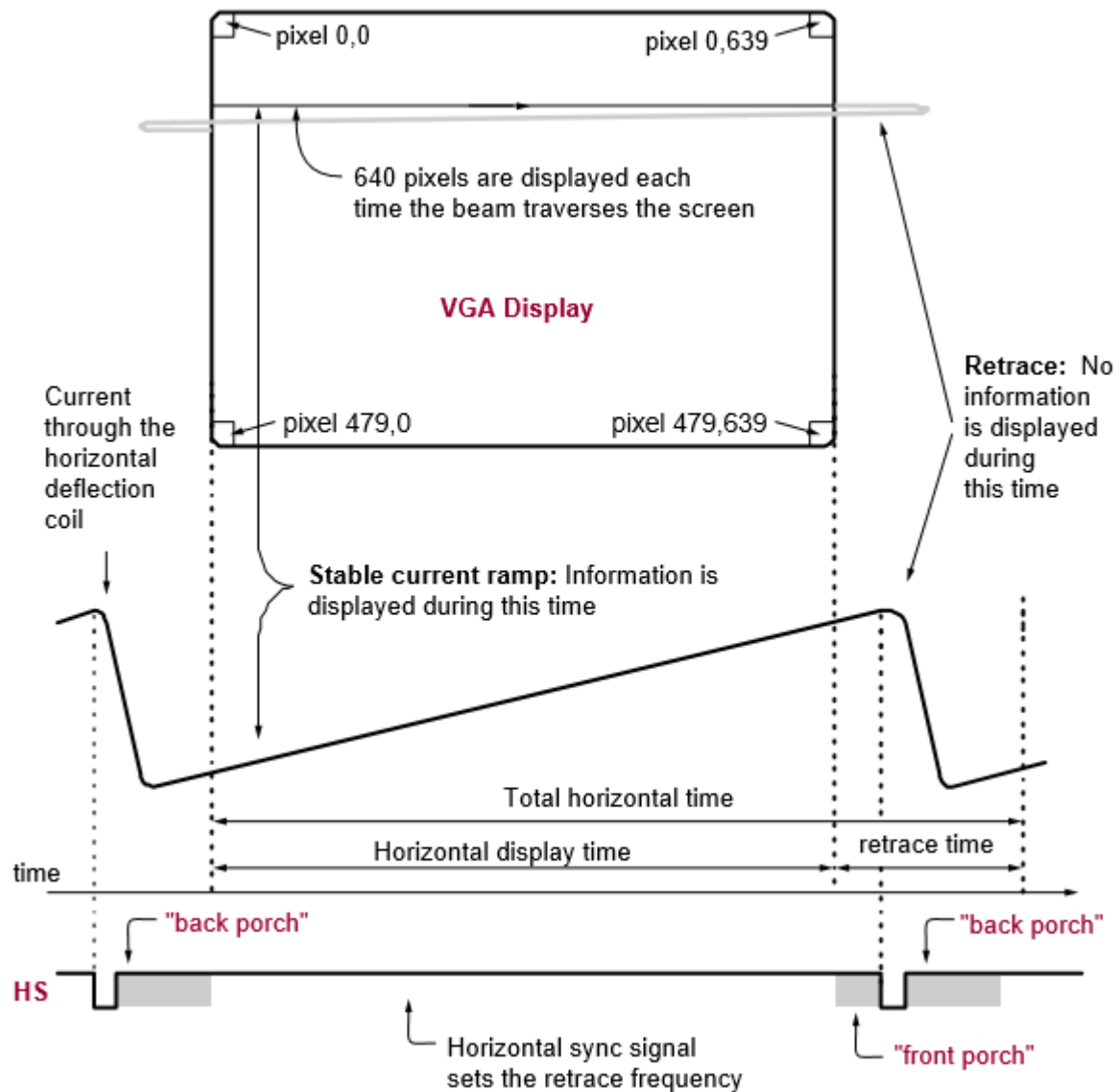
Signal	FPGA Pin
Red (R)	R12
Green (G)	T12
Blue (B)	R11
Horizontal Sync (HS)	R9
Vertical Sync (VS)	T10

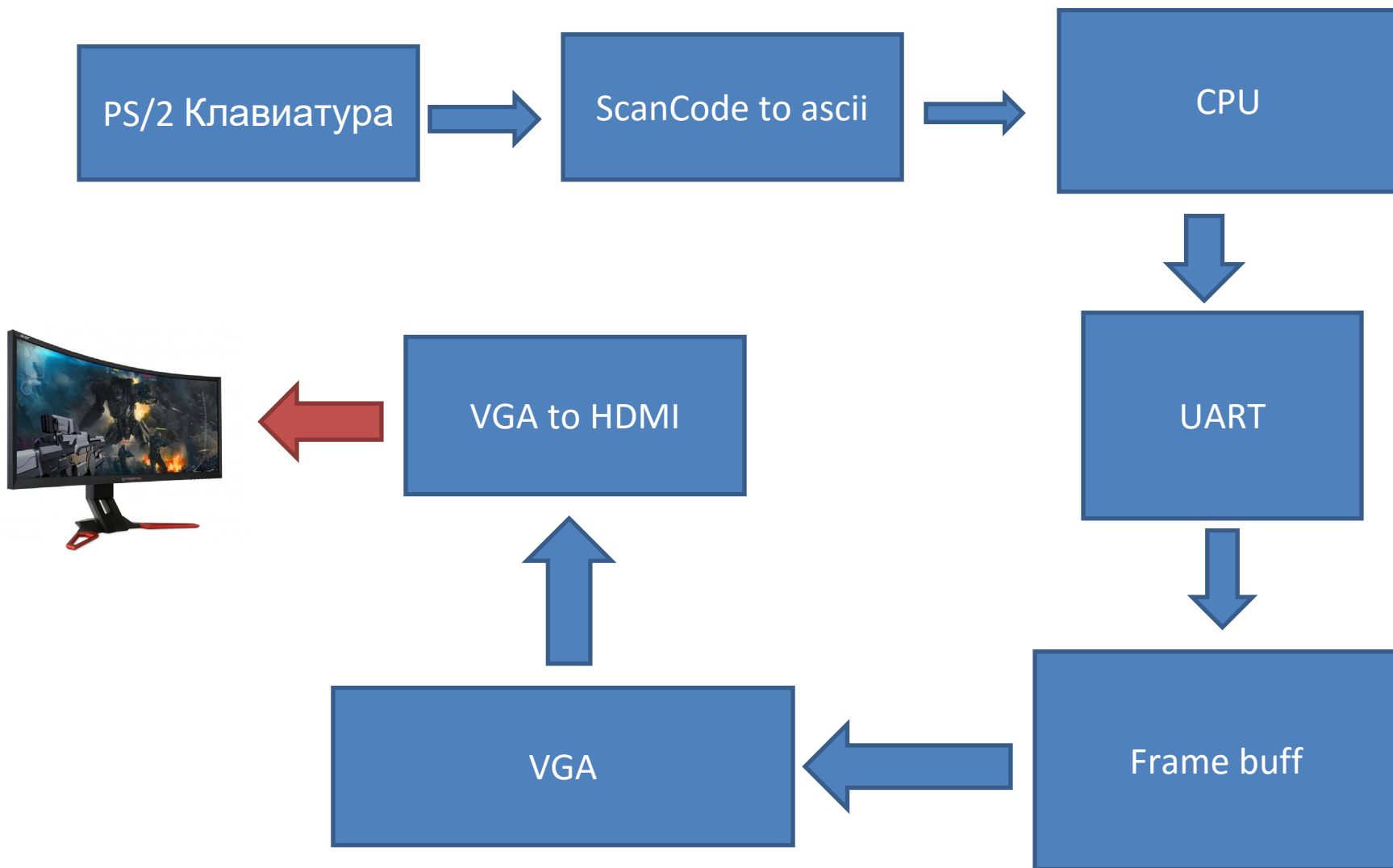


DB15 VGA Connector
(front view)

Red (R)	Green (G)	Blue (B)	Resulting Color
0	0	0	Black
0	0	1	Blue
0	1	0	Green
0	1	1	Cyan
1	0	0	Red
1	0	1	Magenta
1	1	0	Yellow
1	1	1	White







Спасибо за внимание!!!